# Abstracts

## A 5 to 10 GHz low spurious triple tuned type PLL synthesizer driven by frequency converted DDS unit

*K. Tajima, Y. Imai, Y. Kanagawa and K. Itoh. "A 5 to 10 GHz low spurious triple tuned type PLL synthesizer driven by frequency converted DDS unit." 1997 MTT-S International Microwave Symposium Digest 3. (1997 Vol. III [MWSYM]): 1217-1220.*

This paper presents a 5 to 10 GHz low spurious triple tuned type PLL synthesizer with narrow channel steps for wide-band reception in RF measurement systems. The synthesizer is driven by a DDS to achieve such characteristics with a single PLL configuration. It corrects DDS's output frequency and division ratios of two variable frequency dividers in the PLL. With the proposed topology, high level spurious components by the DDS do not fall in from the PLL's loop bandwidth. An added frequency converter placed between the DDS and PLL also suppresses spurious level by reducing a transfer gain from the DDS to the PLL output. Furthermore, a voltage controlled oscillator (VCO) with inverted tuning circuits is presented for low phase noise characteristics. A developed PLL synthesizer with channel step 625 kHz achieved low spurious level below -46 dBc, phase noise of -105 dBc/Hz@1 MHz offset and switching speed of 90 /spl mu/s.

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